IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

VLSI TECHNOLOGY LLC,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Lead Case: 1:19-cv-977-ADA

(*Consolidated with* Nos. 6:19-cv-254-ADA, 6:19-cv-255-ADA, 6:19-cv-256-ADA)

JOINT CLAIM CONSTRUCTION STATEMENT

Pursuant to the Agreed Scheduling Order (D.I. 71) entered in this action, Plaintiff VLSI Technology LLC ("VLSI") and Defendant Intel Corporation ("Intel") submit this Joint Claim Construction Statement.

I. AGREED CONSTRUCTIONS

The parties agree to the following constructions for U.S. Patent No. 7,606,983.

Claim Term	Agreed Construction
"means for accessing data"	**Function:** "accessing data" **Structure:** "a memory circuit, device or system, or equivalents thereof"
"means for processing series of operations and for generating based thereon access requests for the data"	**Function:** "processing series of operations and generating based thereon access requests for the data" **Structure:** "a processor, or equivalents thereof"
"means for controlling access to the data, for receiving the access requests from each of the processing means, for determining a performance order, and for providing the access requests to the accessing means in the performance order"	**Function:** "controlling access to the data, receiving the access requests from each of the processing means, determining a performance order, and providing the access requests to the accessing means in the performance order" **Structure:** "a memory controller, controller for other shared resources, or equivalents thereof"

II. DISPUTED CONSTRUCTIONS

A. U.S. Patent No. 6,366,522 ("The '522 Patent")

Claim Term	VLSI's Construction	Intel's Construction

Claim Term	VLSI's Construction	Intel's Construction
"regulate/regulating at least one supply from a power source and an inductance"	plain and ordinary meaning	"regulate/regulating at least one supply from an inductance connected to a power source, where the inductance is positioned between the power source and the regulating circuitry"

B. U.S. Patent No. 7,292,485 ("The '485 Patent")

Claim Term	VLSI's Construction	Intel's Construction
"a capacitance structure"	plain and ordinary meaning; not means-plus-function	**Function**: providing "capacitance" **Structure**: (1) Dummy column 17 (comprised of dummy SRAM cells 30, 32, and 34 and dummy bitlines SBL and SBL*) and conductor 37, configured to be selectively coupled to one or more of the dummy SRAM cells, as shown in Figure 2, and equivalents thereof; or alternatively (2) dummy row 70 (comprised of dummy SRAM cells 82, 84, and 86 and dummy wordline SWL) and conductor 71, configured to be selectively coupled to one or more dummy of the SRAM cells, as shown in Figure 3, and equivalents thereof

Claim Term	VLSI's Construction	Intel's Construction
"precharging means for precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells"	**Agreed Function:** "precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells" **Structure:** "a conductor, or equivalents thereof"	**Agreed Function:** "precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells" **Structure:** (1) Voltage source V_{REF} and transistor 36, coupled in series to provide a reference voltage to one or more dummy cells through conductor 37, as shown in Figure 2, and equivalents thereof; or alternatively (2) voltage source V_{REF} and transistor 90, coupled in series to provide a reference voltage to one or more dummy cells through conductor 71, as shown in Figure 3, and equivalents thereof

Claim Term	VLSI's Construction	Intel's Construction
"first coupling means for coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells"	**Agreed Function:** "coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells" **Structure:** "a switching circuit, or equivalents thereof"	**Agreed Function:** "coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells" **Structure:** (1) Transistor 52 and clamping circuit 46, configured to couple power supply voltage V_{DD} and conductor 35, as shown in Figure 2 (if the second line of memory cells is SRAM column 15), and equivalents thereof; or alternatively (2) transistor 96 and a clamping circuit, configured to couple power supply voltage V_{DD} and conductor 67, as shown in Figure 3 (if the second line of memory cells is SRAM row 68), and equivalents thereof

Claim Term	VLSI's Construction	Intel's Construction
"second coupling means for coupling the second supply line to the first capacitance structure during the write operation for the second line of memory cells"	**Agreed Function:** "coupling the second supply line to the first capacitance structure during the write operation for the second line of memory cells" **Structure:** "a switching circuit, or equivalents thereof"	**Agreed Function:** "coupling the second supply line to the first capacitance structure during the write operation for the second line of memory cells" **Structure:** (1) Transistor 54, configured to couple conductor 39 to conductor 37, as shown in Figure 2 (if the second line of memory cells is SRAM column 15), and equivalents thereof; or alternatively (2) transistor 94, configured to couple conductor 69 to conductor 71, as shown in Figure 3 (if the second line of memory cells is SRAM row 68), and equivalents thereof
"decoupling means for decoupling the first power supply line from the second line of memory cells during the write operation for the second line of memory cells"	**Agreed Function:** "decoupling the first power supply line from the second line of memory cells during the write operation for the second line of memory cells" **Structure:** "a switching circuit, or equivalents thereof"	**Agreed Function:** "decoupling the first power supply line from the second line of memory cells during the write operation for the second line of memory cells" **Structure:** None, indefinite

C. U.S. Patent No. 7,523,373 ("The '373 Patent")

Claim Term	VLSI's Construction	Intel's Construction

Claim Term	VLSI's Construction	Intel's Construction
"means for providing the operating voltage to the memory at a value at least as great as the minimum operating voltage in response to the operating value selected by the processor being below the minimum operating voltage"	**Function:** "providing the operating voltage to the memory at a value at least as great as the minimum operating voltage in response to the operating value selected by the processor being below the minimum operating voltage" **Structure:** "power supply selector, charge pump, scalable voltage regulator, or equivalents thereof"	Indefinite

D. U.S. Patent No. 7,606,983 ("The '983 Patent")

Claim Term	VLSI's Construction	Intel's Construction
"an indication of a/the specified order"	plain and ordinary meaning	"a second, different indication that indicates a/the specified order"

E. U.S. Patent No. 7,793,025 ("The '025 Patent")

Claim Term	VLSI's Construction	Intel's Construction
"priority level information associated with a [first/second] system mode for each of the one or more interrupt requests"	plain and ordinary meaning	"priority level information associated with a [first/second] system mode for each of the one or more potential interrupt requests"
"priority level information associated with a [first/second] system mode"	plain and ordinary meaning	"priority level information associated with a [first/second] system mode for each of the one or more potential interrupt requests"

Claim Term	VLSI's Construction	Intel's Construction
"storage device for storing priority level information"	plain and ordinary meaning	"hardware for storing priority level information that is not rewritten by software when the system changes mode or context"
"sets of priority levels in … storage devices"	plain and ordinary meaning	"hardware for storing priority levels that are not rewritten by software when the system changes mode or context"
"providing a plurality of interrupt priority storage devices comprising a first interrupt priority storage device for storing priority level information associated with a first system mode, and a second interrupt priority storage device for storing priority level information associated with a second system mode; and providing a plurality of interrupt priority storage devices comprising a first interrupt priority storage device for storing priority level information associated with a first system mode for each of the one or more interrupt requests, and a second interrupt priority storage device for storing priority level information associated with a second system mode for each of the one or more interrupt requests"	Definite	Indefinite

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CERTIFICATE OF SERVICE

A true and correct copy of the foregoing instrument was served or delivered electronically via U.S. District Court [LIVE] — Document Filing System, to all counsel of record, on this 5th day of December, 2019.

/s/ *J. Stephen Ravel*
J. Stephen Ravel